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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/091,776	Applicant(s) KIMURA, KATSUJI	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *12-14 and 22-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 15-21, and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

This application contains claims directed to more than one species of a generic reference voltage circuit type invention. These species are deemed to lack unity of invention because they are not so linked as to form a single general inventive concept under PCT Rule 13.1.

The species are as follows:

Group I: Claims 1-11, 15-21, 26, and claim 27 (the last claim, inadvertently misnumbered originally as claim 20) each require two diode-connected transistors and at least two differential pairs.

Group II: Claims 12-14, and 22-25 only require a single diode-connected transistor, and one differential pair.

The applicant is required, in reply to this action, to elect a single species to which the claims shall be restricted if no generic claim is finally held to be allowable. The reply must also identify the claims readable on the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered non-responsive unless accompanied by an election.

Upon the allowance of a generic claim, if applicable, the applicant will be entitled to consideration of claims to additional species which are written in dependent form or

otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

The claims are deemed to correspond to the species listed above in the following manner:

Each claim is a reference voltage type circuit for generating and outputting a reference voltage. Each claim also requires at least one diode-connected type transistor, and one amplifier.

However, no claim is considered generic.

The species listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, the species lack the same or corresponding special technical features for the following reasons: One group requires two diode-connected type transistors, and at least two amplifiers (for amplifying and summing), wherein the other group requires only a single diode-connected type transistor, and one amplifier.

The applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is considered generic.

The applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument

that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, if applicable, the applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should the applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

During a telephone conversation with the applicant's representative Norman P. Soloway (Reg. No. 24,315) on Dec 13, 2002, a provisional election was made with traverse to prosecute the invention of Group I, claims 1-11, 15-21, and 27. Affirmation of this election must be made by the applicant in replying to this Office action. Claims 12-14, and 22-26 were all originally withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

However, it should be noted that an oversight by the examiner had incorrectly placed claim 26 in with Group II. The oversight was noted when the claims were considered more closely. Since claim 26 depends on claim 16, it still requires two

diode-connected type transistors and two amplifiers. Therefore, the examiner modified the two groups by removing claim 26 from non-elected Group II, and placing it into elected Group I.

Drawings

The drawings are objected to because Fig. 1 shows one amplifier with "11" and "OTA1", and a second amplifier with "12" and "OTA12", wherein the disclosure identifies the amplifiers as "OTA 11" and "OTA 12", respectively. It is suggested the same reference designators be used consistently within the figures and disclosure. Unless Fig. 1 is changed to clearly show "OTA 11" and "OTA 12", it is suggested "OTA 11" be changed to --OTA1 11-- on pages 14 (line 14) and 17 (lines 21 and 23), and "OTA 12" be changed to --OTA2 12-- on pages 14 (lines 17 and 20) and 18 (lines 3 (two occurrences), 4, and 6). Figs. 5 and 6 should show transistor M2 in the same manner as all the other FETs, because M2 could be mistaken as a JFET as presently shown. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "M5" has been used to designate both a current source to differential pair M1,M2, and as a transistor coupled between an input and output of the differential pair in Fig 8. When those duplicate reference designators are corrected, their associated descriptions on pages 41-42 (e.g. see page 41, lines 13-14 and 21) must also be changed accordingly. Also related to the same reference characters being

used for different elements, 1) Fig. 1 shows transistors M1-M3 forming a current mirror, wherein Figs. 5, 6, and 9 each show them as input transistors of differential pairs; 2) Figs. 5 and 6 each show transistors M5 and M6 as input transistors of a differential pair, wherein Fig. 7 shows them in a current mirror; and 3) Figs. 8 and 9 show transistors M3 and M4 as an active load/current mirror, while each of Figs. 5-7 show them as input transistors of a differential pair. Therefore, the figures, and their descriptions, should be modified to ensure no reference character is used more than once, unless the element is shown in the same consistent manner (e.g. a designator of a differential pair's input transistor will always identify such an input transistor throughout the application). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "M15" and "M14" are not shown in Fig. 8, although they are described on page 46, lines 2-4. However, it is believed the description meant --M13 -- and --M12--. A proposed drawing correction, corrected drawings, or corrected description are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 11, line 14 "isK3:1" should be --is K3:1--. Page 16, lines 24-25 "M11 having its gate connected

to the drain of the MOS transistor M11 and a current mirror circuit" since neither Fig. 8 or 9 shows the gate and drain of M11 being coupled together. However, the gate is coupled to current mirror M12,M13 through R1, and the drain is coupled directly to the current mirror in both figures. Page 17, line 23 "Q" should be --Q1--. Page 18, line 19 "VBE" should be --VBE1-- to correspond to the designation on line 21. Page 30, line 23 "MP(K2+4)3" needs clarification. For example, was --MP(K2+4)-- meant? Page 31, line 3 "MN(K2+1)" should be --MN0(K2+3)-- to correspond to the transistor shown in Fig. 6. Page 31, line 7 "MN02" should be --MN2-- since the drain connection is now referring to the differential pair transistor. Page 32, line 2 "M (2K+2)" should be --M(2K2+2)--, and "MP (2K+1) and MP(2K2+2)" on line 15 should be --M(2K2+1) and M(2K2+2) --, to be consistent with Fig. 6's reference designators. Similarly, "MN10" (pages 35 (line 24) and 36 (line 2)) should be --M10--, and "MN11" (page 36, line 2) should be --M11-- to correspond to Fig. 7. Although M1 can be considered one type of a current source, it is suggested "current source" on line 15 of page 41 be deleted to correspond with previous descriptions of M1. Page 41, lines 19-21 need clarification. For example, does the description refer to the drain of "M2" or --M4--, since M4 has the grounded source? (However, it is understood that the drain of M2 can be considered grounded through M4.) Page 52, line 11 "constructed measly by" needs clarification. Appropriate corrections are required.

Claim Objections

In the original numbering of the claims, the claim (i.e. the last claim) following claim 26 was inadvertently misnumbered as claim 20. However, it has now been

renumbered as --27-- in accordance with 35 CFR 1.126, and has been referred to as claim 27 in this action.

Claims 1-11, 15-21, 26, and 27 are objected to because of the following informalities: The phrase "an output voltage" in claim 1 (lines 8-9 and 16) should be --the output voltage-- since the voltage is understood to relate to "outputs voltages of said...transistors" already recited on lines 6-7. Similarly, "an output voltage" on lines 8-9 and 15 of claim 5; lines 8-9 and 15 of claim 6; and lines 8-9 and 14 of claim 7 should be --the output voltage-- since the voltage is understood to relate to the previously recited "output voltages of said first and second diode-connected transistors." To help clarify that no other limitations were intended within claim 2, it is suggested --and-- be added after "gm2);" on line 3. For consistent labeling throughout the claims, it is suggested "that" on line 4 of claim 3 be changed to --the transconductance--. To improve word flow within each of claim 5, and to use labeling more consistent within the claims, it is suggested "of differential pair transistors" on line 14 be changed to --transistor--; and "of said differential pair transistors" on line 16 be changed to --transistor of the second differential pair--. Similarly, it is suggested claim 6 has "of differential pair transistors" on line 14 changed to --transistor--; and "of said differential transistors" on line 16 be changed to --transistor of the second differential pair--. Although claim 9 recites "K1 times", and claim 10 recites both "K2 times" and "K3 times", each claim should clarify what their respective "K1", "K2", and "K3" relates to. It is suggested "are" on line 22 of claim 16 be changed to --is-- since it refers to the singular subject "a connection node." Claim 17 should clarify what "VBE2" and "ΔVBE2"

represent on line 23. Since "base-to-emitter voltages of said first and second bipolar transistors" were already recited on lines 7-8 of claim 18, it is suggested "a base-to-emitter" on line 16 be changed to --the base-to-emitter-- within the same claim. It is also suggested "a drain" and "the MOS" on claim 18's line 27 be changed to --the drain-- and --the other MOS--, respectively to correspond to the "other MOS transistor" and "drain" previously recited on lines 25-26. For the same reasoning as applied to claim 18 above, it is suggested "a base-to-emitter" on line 20 of claim 19 be changed to --the base-to-emitter--. Since the second current mirror circuit has the output ends, it is suggested --second-- be added prior to "current mirror circuit" on line 23 of claim 19 to ensure it won't be confused with the first current mirror circuit. Both claims 20 and 27 should clarify what "VBE2" and "ΔVBE2" represent on line 19. For the same reasoning as applied to claims 18 and 20 above, it is suggested "a base-to-emitter" on claim 21's line 15 be changed to --the base-to-emitter--.

Dependent claims carry over rejection(s) from claims upon which they depend. Appropriate corrections are required.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See

MPEP § 2172.01. The omitted structural cooperative relationships are: how the current mirror circuit relates to either OTA within the amplifying/summing means.

Claims 5, 6, 8-11, 15-21, 26, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention as described below. The limitation cited on line 12 of claim 5 makes the claim indefinite when K2 is equal to 1. For example, when K2 is equal to 1, there are only two pairs. However, line 21 specifically identifies a "third" pair. Therefore, it is believed "1" on line 12 was meant to be --2 --. For similar reasons, "K2" within claim 6 (e.g. line 11) is not clearly identified with respect to what it represents, and needs to be at least equal to 2 to ensure there is at least a "third" differential pair (e.g. see line 18). It is not clear in claim 8, line 4 how "two constant currents" relate to the "two constant currents" recited on line 19 of claim 7. For example, are the currents related to the differential pairs or to current through the first/ second diode-connected transistors? Similarly, how does "the driving current ratio" on line 3 of both claims 9 and 10 relate to the "constant current ratio" of claim 7, and/or the currents that flow through the differential pairs, and any current that will flow through the first/second diode-connected transistors? It is not clear what "a diode is employed as said diode-connected transistor" means in claim 15. For example, claim 1 cites first and second diode-connected transistors, but claim 15 implies there is only one. Also, if either diode-connected transistor of claim 1 is replaced by a simple diode, then claim 1's limitation of "first and second diode-connected transistors" is no longer valid because then there will be only one diode-connected transistor. On lines 3-4 of each of claims

16, 18, 19 and 21, the phrase "each collector being fed with a constant current" is misleading. None of the applicant's own figures shows both collectors coupled in common to receive a single current. Was --each collector being fed with a respective constant current-- meant? Related to this, what does "the same constant current is" mean on line 4 of claim 17? For example, was --the respective constant currents are equal, and are-- meant? It is not clear if all the intended limitations have been recited within claim 17 since it lacks an --and--. For example, do the limitations within claim 17 refer to any one of the emitter area sections recited on lines 2-14, and still include the rest of the limitations recited on lines 15-23? It appears --and wherein-- may have been intended to be cited after "different from 1;" on line 14 of claim 17. [Claim 17 would then correspond to the similarly recited limitations within at least claim 20.] It is not clear how "a constant current" on lines 4, 6, 15, and 22 of claim 18 relate to one another. It is not understood in claim 18 how the singular "said differential pair" on lines 22 and 25 relate to the first through (K2+1) differential pairs recited within the claim. For example, was --each of said third to number (K2+1) differential pairs-- meant? It is not understood how "a constant current" on lines 4, 6, 15, 19, 25-26, and 40-41 of claim 19 relate to one another. Similar to claim 18 above, it is not clear in claim 19 how the singular "said differential pair" on lines 27 and 33 relate to the first through number K2 differential pairs recited within the claim. For example, was --each of said third to number K2 differential pairs-- meant? Claim 19, line 39 "a number (K2+1) differential pair, each comprised" is confusing because "pair" is singular, while "each" implies more than two. Therefore, is there more than one "number (K2+1) differential pair"? The drain connection to the first

current mirror circuit's output end is confusing in claim 19, lines 44-46. For example, it appears the drain refers to the drain of the "other transistor of the number K2 differential pair", which is connected to the drain of the "one of the MOS transistors" within the (K2+1) differential pair. However, that connection does not correspond to the applicant's own figures. It is actually believed the (K2+1) differential pair corresponds to pair M(2K2+1),M(2K2+1) of the applicant's Fig. 6, wherein the drain of the other MOS transistor M(2K2+2) is coupled to the output end MN03 of the first current mirror circuit MN02,MN03. Similar to claim 17, each of claims 20 and 27 has the same problem with respect to "the same constant current" (line 4). It is not clear if "the reference voltage output" on line 18 of claim 20 refers to "a reference voltage being taken out" recited on line 27 of claim 18. For example, the voltage is from the "(K2+1)" pair in claim 18 (lines 27-28), but claim 20 has it from the "K2" pair. It is not understood how "a constant current" on lines 4, 6, and 14 relate to one another in claim 21. It is not clear what "a cathode-grounded diode in place as said emitter-grounded bipolar transistor" means in claim 26. For example, claim 26 cites first and second emitter-grounded bipolar transistors, but claim 26 implies there is only one. Also, if either emitter-grounded bipolar transistor of claim 16 is replaced by a simple cathode-grounded diode, then claim 16's limitation of "first and second emitter-grounded bipolar transistors" is no longer valid because then there will be only one emitter-grounded bipolar transistor. It is not clear if "the reference voltage output" on line 18 of claim 27 refers to "a reference voltage being taken out" recited on lines 45-46 of claim 19. For example, the output

voltage is believed to be from the "(K2+1)" pair in claim 19 (lines 39-47), but claim 27 has it from the "K2" pair.

Claim 11 recites the limitation "said third differential pair" in line 7. There is insufficient antecedent basis for this limitation in the claim because claim 7 only recites first and second differential pairs.

Each of claims 17, 20, and 27 recite the limitation "the respective constant currents" in line 7 with insufficient antecedent basis for this limitation in the claim. For example, this relates to the previously described problems with respect to "a constant current" (lines 3-4 of respective claims 16, 18, and 19) and "the same constant current" (line 4 of respective claims 17, 20, and 27).

Dependent claims carry over rejection(s) from any rejection claim upon which they depend.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In so far as being understood, claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by McNeill et al. (McNeill). McNeill shows a CMOS reference voltage circuit in Fig. 1 comprising first/second diode-connected transistors Q1/Q2 being respectively driven by two constant currents 10μA/80μA with a constant current ratio (i.e. 1:8). The figure also shows what can be deemed a means for

amplifying and summing 112,M3,170,116. The means comprises first/second operational transconductance amplifiers (OTAs) 112/116, and a current mirror circuit 170. The first OTA 112 receives the differential voltage (i.e. N1 and N2); the second OTA 116 has a first input terminal + receiving output voltage N2 from the second diode-connected transistor Q2, and a second input terminal - connected to output terminal N4 of second OTA 116 that is driven with current (through M3 and 170) proportional to output current of first OTA 112, wherein output terminal voltage VBG of second OTA 116 is the reference voltage VBG. Therefore, claim 1 is anticipated. Since both transistors Q1 and Q2 are diode configured, they can each be deemed a diode, anticipating claim 15. [Also, it is noted that McNeill discloses other diode junction devices could be used, such as diodes, on column 3, lines 50-56.]

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 16 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McNeill et al. (McNeill). Fig. 1 of McNeill shows a reference voltage circuit comprising first/second bipolar transistors Q1/Q2, each having its base connected to its collector, and each receiving a respective constant current (i.e. 10μA or 80μA); first/second operational conductance amplifiers (OTAs) 112/116, each having first/second input terminals -/+ and adapted to output a current proportional to a

differential voltage applied to the input terminals (e.g. a current is known to be proportional to voltage); and current mirror 170 having an input end M4 and an output end M5 with a predetermined current ratio of 1:1 (i.e. M5=M4). The output terminal of first OTA 112 is connected to input end M4 through M3; a connection node N3 is connected to first input terminal - of second OTA 116, output terminal N4 of second OTA 116, and output end M5 of current mirror circuit 170, wherein output terminal N4 outputs reference voltage VBG. However, the reference does not show the diode-connected transistors Q1 and Q2 as emitter-grounded bipolar transistors. McNeill discloses bipolar PNP transistors 106 and 108 are diode junctions, and NPN bipolar transistors, and other semiconductor devices (e.g. diodes or MOS devices) could also be used to provide those diode junctions. Therefore, it would have been obvious to one of ordinary skill in the art to replace each of diode-connected PNP transistors Q1,Q2 of McNeill with corresponding diode-connected NPN transistors. In that case, the first/second diode-connected NPN transistors Q1/Q2 will each have its base and collector connected together, and its emitter connected to ground V_{SS}. With this type of configuration, the collectors of the first/second diode-connected NPN transistors will be connected to their respective input terminal of first OTA 112; and output terminal N4 of second OTA 116 and the collector of second bipolar transistor Q2 will be connected to the first/second input terminals of second OTA 116, respectively. Therefore, claim 16 is rendered obvious. Replacing diode-connected PNP transistors with diode-connected NPN transistors is one known way to still provide a diode junction where necessary. Whether first/second transistors are diode-connected PNP, NPN, PMOS, or NMOS

transistors, or simple diodes, they will still have a grounded cathode, thus rendering claim 26 obvious. For example, to forward bias a diode junction, the anode is coupled to a higher voltage potential than its cathode, wherein the junction will begin to conduct once the voltage potential across the diode junction passes the junction's trigger point. Since diode-connected bipolar transistors Q1/Q2 use ground V_{SS} as the lower potential, the cathode of the diode-junction will be grounded.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 2-11, 17-21, and 27 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office Action and to include all of the limitations of the base claim and any intervening claims, where applicable. There is no motivation to modify or combine any prior art reference(s) to ensure the circuit comprises the first/second diode-connected transistors, and a means of amplifying and summing, wherein the means comprises at least: 1) the first/second operational transconductance amplifiers and current mirror circuit as recited within claims 2-4, wherein "K2 > 1"; 2) the "(K2+1) differential pairs" as recited within claim 5, wherein the other transistors within each of the second to K2 pairs are diode-connected, and the differential input voltages of the second to (K2+1) differential pairs are summed together; and 3) the "(K2+1) differential pairs" as recited within claim 6, wherein the transistors within each of the third to K2 pairs are diode-connected, and the differential input voltages of the second to (K2+1) differential pairs are summed together; 4) the second differential pair has a diode-connected transistor, and the operating input

voltage range of the second differential pair is a predetermined number multiple of the first differential pair's operating input voltage range as recited within claim 7 (upon which claims 8-11 depend). Similarly, there is no motivation to modify or combine any prior art reference(s) to ensure the circuit comprises the relationships between the first/second bipolar transistors (each having a respective base connected to a respective collector to form a diode-connected transistor), and: 5) the reference voltage output is given by VBE2 + (K2 X ΔVBE2 X gm1)/gm2 as recited within claim 17; 6) the first to number (K2+1) differential pairs, with gate-to-drain connected MOS transistors, and the current mirror circuit as recited within independent claims 18 (upon which claim 20 depends) and 19 (upon which the last claim 27 (inadvertently identified as another claim 20) depends); and 7) the first/second differential pairs and current mirror circuit as recited within independent claim 21, wherein the second differential pair has a drain-to-gate connected MOS transistor.

Claims 12-14, and 22-25 were withdrawn from consideration because they only require one diode-connected transistor, and one differential pair, wherein the elected claims 1-11, 15-21, and 26-27 each require two diode-connected transistors, and at least two differential pairs.

Prior Art

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although each of the references show either two diodes or diode-connected bipolar transistors, along with two differential pairs (e.g. amplifiers), none of these references show or disclose more than two

differential pairs, or even a transistor within the differential pair as being diode-connected, as recited within some of the claims. Also, the references of Kotowski and Salter et al. both lack a current mirror in the circuit shown with the two differential pairs, and two diodes (or diode-connected transistors). However, some other differences in each reference will now be described: 1) The second OTA 16 of Bitting's Fig. 3 does not have an input coupled to its output, or to one of the two diode-connected transistors 2 coupled to the inputs of first OTA 9; and neither of the differential pairs shown in Figs. 4 and 5 show the "other" transistor as being diode-connected; 2) Fig. 10 of Kotowski does not show/disclose diode-connected transistors; a current mirror; or the second OTA 80 having its output coupled to one of its inputs (excluding the inverse input and output terminals both being coupled to ground); and 3) Salter et al.'s Fig. 6 lacks a current mirror between the two OTAs 608,614; the output of second OTA 614 is not coupled directly to one of its inputs; and details of the OTAs are not shown. Although these references do not read on the limitations recited within the present claims, as presently understood, the references (including McNeill et al.) should be carefully reviewed and considered do to their utilization of at least the two amplifiers and two diodes (or diode-connected transistors).

The prior art reference cited on the IDS submitted Mar 5, 2002 lacks the at least two OTAs (e.g. differential pairs) as recited within each of the examined claims.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

10 February 2003

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